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PATENT
8017-1189

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Shinji WATANABE et al. Conf. 3401

Application No. 10/574,898 Group 2814

Filed April 6, 2006 Examiner Thao X. Le

ELECTRONIC DEVICE AND MANUFACTURING METHOD OF THE SAME

REQUEST FOR CORRECTED OFFICIAL ACTION

Assistant Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

September 5, 2007

Sir:

The Official Action of August 21, 2007 does not seem to be correct. It acts on claims 1-25. In fact, the claims in the case are 17-37, as established by the Preliminary Amendment filed April 6, 2006. Another copy of that Preliminary Amendment is enclosed, with a copy of the receipt card proving its filing.

Kindly send to us a correct Official Action and set a new period for response.

Respectfully submitted,

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INT. APPLN. # PCT/JP2006/014739 Doc' No. 8017-1189

ATTACHED IS A NEW NATIONAL PHASE APPLICATION OF

INVENTOR(S): Shinji WATANABE and Yukio YAMAGUCHI

TITLE: ELECTRONIC DEVICE AND MANUFACTURING METHOD OF THE SAME

FILING DATE: April 6, 2006

CONSISTING OF: ☒ Transmittal Letter (PTO-1390) ☐ SMALL ENTITY CLAIM

☒ Published Application (Non-English) ☒ English Language Translation

44 Total pages consisting of **29** Pages of Description, 4 Pages of Claims

10 Sheets Of Drawings and 1 Page(s) Abstract

☒ Application Data Sheet	☐ PCT/IB/308
☒ Preliminary Amendment	☐ Coversheet of Publication
☒ Executed declaration (1)	☒ Exec. Assignment w/PTO-1595
☐ Paper Sequence Listing	☐ Computer readable Seq. List. (diskette)
☐ Not. of Sub. of Sequence Listing	☐ Article 19 Amendments
☐ International Preliminary Examination Report (PCT/IPEA/409)	
☐ Amended sheets w/IPER	☐ Confirmation of §1.78 Submission
☒ Info. Disclosure Statement w/1449	☒ International Search Report
☒ 13 Cited References	☒ Check # **34719** for $**$990.00**

Other:_____

USPTO - PLEASE STAMP RECEIPT DATE AND APPLICATION NUMBER

Actual due date: **4/6/2006** BC/ia

PATENT
8017-1189

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Shinji WATANABE et al. Conf.

Application No. **NEW NATIONAL PHASE** Group

Filed April 6, 2006 Examiner

ELECTRONIC DEVICE AND MANUFACTURING METHOD OF THE SAME

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 6, 2006

Sir:

The following preliminary amendments and remarks are respectfully submitted in connection with the above-identified application.

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.

Remarks begin on page 7 of this paper.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1-16 (cancelled)

17. (new) An electronic device comprising:

a wiring substrate including an insulating resin layer having a first major surface and a second major surface and a first wiring layer disposed on said insulating resin layer on the second major surface side;

a second wiring layer formed on the first major surface of said insulating resin layer;

a chip part including a projection electrode on a bottom surface and mounted on said wiring substrate; and

wherein said insulating resin layer holds said chip part such that a bottom and at least a part of side surfaces of said chip part are in contact with said insulating resin layer, and a top surface of said chip part is exposed on said insulating resin layer on the first major surface side, and wherein the projection electrode of the chip part is connected with said first wiring layer.

18. (new) The electronic device according to Claim 17, wherein said chip part protrudes from the first main major surface of said insulating resin layer.

19. (new) The electronic device according to Claim 17, wherein a ground pattern is formed in said second wiring layer.

20. (new) The electronic device according to Claim 17, further comprising a plurality of insulating resin layers for holding the chip part.

21. (new) The electronic device according to Claim 20, wherein the insulating resin layers for holding the chip part are laminated such that the first major surfaces are faced in the same direction.

22. (new) The electronic device according to Claim 17, wherein said insulating resin layers for holding said chip part are arranged on both surfaces of said wiring substrate.

23. (new) An electronic device comprising:

a wiring substrate including a plurality of insulating resin layers that are laminated and have first major surfaces and second major surfaces and a first wiring layer disposed on said insulating resin layer on the second major surface side from a lowermost layer to an innermost layer in said resin insulating layers;

a second wiring layer formed on the first major surface of said insulating resin layer;

a chip part including a projection electrode on a bottom surface and mounted on said wiring substrate; and

wherein said insulating resin layer holds said chip part such that a bottom and side surfaces of said chip part are in contact with said insulating resin layer in a outmost layer, and a top surface of said chip part is exposed on said insulating resin layer on the second major surface side, and wherein the projection electrode of the chip part is connected with said first wiring layer.

24. (new) The electronic device according to Claim 17, wherein said wiring substrate further comprises an insulating

layer except for said insulating resin layer and further comprises a wiring layer except for said first wiring layer or first and second wiring layers.

25. (new) The electronic device according to Claim 17, wherein a portion exposed from the insulating resin layer of the chip part that enters the insulating resin layer of the outmost layer in the wiring substrate, is covered by a coating resin.

26. (new) The electronic device according to Claim 17, wherein the projection electrode of said chip part is provided with a portion having a sharp tip.

27. (new) The electronic device according to Claim 17, wherein the projection electrode of said chip part is a gold electrode formed by a wire bonding technique.

28. (new) The electronic device according to Claim 17, wherein said insulating resin layer is made of thermoplastic resin or materials in which thermosetting resin is added to thermoplastic resin.

29. (new) A method of manufacturing an electronic device, comprising the steps of:

preparing a wiring substrate having an insulating resin layer having a first major surface and a second major surface, a first wiring layer disposed on said insulating resin layer on the second major surface side and a second wiring layer disposed on said insulating resin layer on the first major surface side, and a chip part including a projection electrode;

pushing the chip part into the insulating resin layer from the first major surface; and

passing the projection electrode of the chip part through the insulating resin layer to be connected with the first wiring layer and sealing at least a surface on which the projection electrode of the chip part is formed with resin of the insulating resin layer.

30. (new) The method according to Claim 29, wherein the step of pushing said chip part comprises pushing said chip part while heat is applied.

31. (new) The method according to Claim 29, wherein the step of pushing said chip part comprises pushing said chip part while ultrasonic vibration is applied to said chip part or to said wiring substrate.

32. (new) The method according to Claim 29, further comprising a step of applying a plasma process or ultraviolet ray irradiation to at least a portion that is to be pushed by said chip part on to the first major surface of said insulating resin layer before the step of pushing said chip part.

33. (new) The electronic device according to Claim 23, wherein said wiring substrate further comprises an insulating layer except for said insulating resin layer and further comprises a wiring layer except for said first wiring layer or first and second wiring layers.

34. (new) The electronic device according to Claim 23, wherein a portion exposed from the insulating resin layer of the chip part that enters the insulating resin layer of the outmost layer in the wiring substrate, is covered by a coating resin.

35. (new) The electronic device according to Claim 23, wherein the projection electrode of said chip part is provided with a portion having a sharp tip.

36. (new) The electronic device according to Claim 23, wherein the projection electrode of said chip part is a gold electrode formed by a wire bonding technique.

37. (new) The electronic device according to Claim 23, wherein said insulating resin layer is made of thermoplastic resin or materials in which thermosetting resin is added to thermoplastic resin.

REMARKS

Claims 17-37 remain in this application. Claims 1-16 have been canceled. Claims 17-37 has been added.

Entry of the above amendments is earnestly solicited. An early and favorable first action on the merits is earnestly requested.

Should there be any matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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